REMARKS

The drawings were objected to by the PTO draft person for the reasons noted on the form PTO-948. The applicants have filed informal drawings with the application. The formal drawings will be filed after receiving a notice of allowance.

The Examiner objected to the boxes in Figure 2 and the terminals of Figures 1 and 2 as being "not labeled as their functions." The Applicant respectfully traverses the objections. The Applicant respectfully submits that the application sufficiently describes the Figures 1 and 2 for the purposes of the present invention, and respectfully requests that the Examiner withdraw the objections or provide reasons and legal citations for the requirement. According to the Rules, the drawings "should contain as few words as possible." 37 CFR 41.81(o), MPEP 608.02.

The disclosure is objected to purportedly because of informalities. The Examiner requests modification of the article preceding the dependent claims 2, 3, 5-10, 12, 13, 15, and 18 from indefinite articles "A" or "An" to the definite article "The". The Applicant respectfully traverses the objection. The Applicant respectfully submits that the form of the above-listed dependent claims is proper. In particular, the Applicant respectfully submits that the use of the indefinite articles "A" and "An" is proper. See MPEP 608.01(n).

The Specification was objected to for purportedly failing to provide antecedent basis for the "noise detector circuit" of Claim 9. Office Action p. 2. The Applicant respectfully submits that Claim 9 does not recite a "noise detector circuit."

Claim 11 has been amended to recite "noise separator circuit" rather than "noise detector circuit." The "noise separator circuit" is discussed, *inter alia*, on page 8 of the present Specification.

Claims 1 through 19 were rejected under 35 U.S.C. 112, first paragraph. The Applicant respectfully traverses this rejection.

As for claims 1 and 4, the Examiner states that "it is not understood how the second circuit is designed to have equal noise to the first circuit or to produce noise only." Office Action p. 3. The second circuit produces noise equal to the noise of the first circuit because the second circuit is identical in design to the first circuit, thereby having the same noise characteristics, and is placed proximal to the first circuit so as to experience the same environmental noise affecting the first circuit. This concept is clearly discussed by the Specification. See, *inter alia*, p. 5, ll. 21-23.

As for claim 7, the Examiner misquotes claim 7 as having the phrase "second circuit can be an inverse function of said first circuit". Claim 7 states that, because the second circuit is identical to the first circuit, a second input, inverse of the first input, causes said second circuit to produce an output which is the inverse of the output of the first circuit, plus noise.

As for claim 9, the Applicant respectfully submits that "noise detector circuit" is not an element of claim 9. Claim 11 has been amended to recite "noise separator circuit," not a "noise detector circuit."

As for the remaining claims, the Examiner failed to specify the reasons for which the remaining claims were rejected under 35 U.S.C. 112, first paragraph.

Claims 1-19 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Applicant respectfully traverses the rejection.

As for Claims 1, 4, and 7, the Office Action states that "first function" is vague and indefinite. The Applicant respectfully submits "first function" is not recited by claims 1, 4, or 7.

Claims 1, 4, and 7 were rejected because purportedly "it is not clear where the 'noise component' is from" and how the first circuit can include the noise. The source of the noises of the circuits are succinctly described, *inter alia*, on pages 1 and 2 of the Specification.

As for claims 3, 8, 14, and 18, the Office Action states that "it is not understood what the 'halving' circuit' is." The Applicant respectfully submits that halving circuits are well known in the art. The Office Action itself states that "the halving circuit function as a substructor is notoriously well known in the art." Office Action page 4. The specification discusses the use of "notoriously well known" halving circuits on pages 7 and 8.

Further, as for claims 3, 8, 14, and 18, the Office Action states that "it is not understood... how the substructor can be the halving circuit." The Applicant respectfully submits that halving circuits are well known in the art. The Office Action itself states that "the halving circuit function as a substructor is notoriously well known in the art." Office Action page 4. The specification discusses the use of "notoriously well known" halving circuits on pages 7 and 8. In

any event, none of the listed claims state that the substructor circuit "can be" the halving circuit. The Applicants respectfully submit that it would be a mischaracterization of the present application to claim that the application claims a substructor as a halving circuit.

As for claim 4, the Office Action states that "it is not understood how the second circuit is designed." Claim 4 expressly states that the second circuit is identical to said first circuit. As for the second input, please see the last paragraph of page 6 of the Specification. The Applicant respectfully submits that the word "design" is not indefinite, and is supported by the Specification. However, in deference to the Examiner, the Applicant has amended claim 4 to remove the word "design."

The Office Action specifies several reasons for rejecting claim 11. First, the Office Action states that "it is not understood how the noise canceling circuit can process the outputs from the plurality of analog circuits. A preferred embodiment of the noise canceling circuit is shown by Figure 2 and discussed, *inter alia*, as substructor circuits on page 8, last paragraph. Secondly, the Office Action states that "[i]t is unclear how the recitations" of the recited elements are read on the preferred embodiment and asserts that no such means are seen in the drawings. Recitations of claim 11 are shown in Figure 2 and are discussed on, *inter alia*, pages 8 and 9 of the Specification. Thirdly, the Office Action asserts that "description of the present invention is incomplete because the claim fails to provide an input/output." The Applicant respectfully submits that the description of the present invention is complete and there are no requirements to provide "an input/output." The Applicant respectfully requests that the

Examiner point out the specific sections of the Code, the Rules, or the MPEP requiring recitation of "an input/output" in the present context.

As for claim 14, the act of "reading" a signal is defined as obtaining the signal for further processing as discussed on page 3, paragraph 3 of the Specification.

As for claims 14, 18, and 19, the Office Action inquires as to what "null signal" is. Null input signal is defined as a zero input or a signal which causes the noise separator circuit to produce the noise component only. See page 9 of the Specification.

Claim 17 does not recite "said added output"; therefore it requires no antecedent basis for such element.

Claim 18 recites "said added output." The "added output" is found in claim 17 in the clause "adding said second output to said first output."

The remaining claims were rejected under 35 U.S.C. 112, second paragraph, due to the purported deficiencies of claims 1, 4, 7, and 14. As discussed, the Applicant respectfully submits that the remaining claims are definite in light of the above discussion overcoming the purported deficiencies of claims 1, 4, 7, and 14.

Claim 1 was rejected under 35 U.S.C. 102(b) as being anticipated by IBM Disclosure Bulletin (Vol. 28, No. 9, February 1996, page 3981) (the "IBM reference"). The Applicant respectfully traverses the rejection. The Office Action asserts that the first circuit, the second circuit and the subtractor as recited in claim 1 are anticipated, respectively, by the flip flops (S74) and the EXCLUSIVE OR gate S86. The Applicant respectfully submits that the flip

flops and the EXCLUSIVE OR gate does not anticipate the first circuit, the second circuit, and the subtractor circuit of claim 1. The first circuit of claim 1 requires a first input and a first output wherein said first output is a function of said first input plus noise. Contrary to the first circuit, the first flip flop of the IBM reference having input (A) and output (B) does not have an output which is a function of its input (A) plus noise component. In fact, the output (B) of the first flip flop of the IBM reference is a function of an input (A) and its own output (B) which is fed back into the first flip flop. Moreover, output (B) has no noise component. As for the second circuit of claim 1, the second flip flop of the IBM reference having input (a) and having output (C) is not required to be located proximal to the first flip flop. And, the second input (a) does not cause the second output (C) to equal the noise component of the first output (B). Moreover, the EXCLUSIVE OR (XOR) gate of the IBM reference is not a subtractor circuit as recited in claim 1. The XOR gate of the IBM reference does not subtract the second output (C) from the first output (B).

Claim 2 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. The Applicant respectfully submits that claim 2 is not anticipated by the IBM reference for the same reasons for which claim 1 is not anticipated by the IBM reference.

Claim 3 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. However, the Examiner failed to provide reasons for which claim 3 was being rejected including the particular part relied upon for the rejection of claim 3. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does

not anticipate claim 3 for the same reasons for which the IBM reference does not anticipate claim 1. Moreover, the Applicant respectfully submits that the IBM reference does not anticipate claim 3 because the IBM reference does not include a halving circuit, as recited by claim 3.

Claim 4 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. However, the Examiner failed to provide reasons for which claim 4 was being rejected including the particular part relied upon for the rejection of claim 4. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that claim 4 is not anticipated by the IBM reference for the same reasons for which claim 1 is not anticipated by the IBM reference.

Claim 5 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. However, the Examiner failed to provide reasons for which claim 5 was being rejected including the particular part relied upon for the rejection of claim 5. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 5 for the same reasons for which the IBM reference does not anticipate claim 4 and for the same reasons for which the IBM reference does not anticipate claim 2.

Claim 7 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. However, the Examiner failed to provide reasons for which claim 7 was being rejected including the particular part relied upon for the rejection of claim 7. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 7 for the same reasons for which the IBM reference does not anticipate claim 1. In addition, the second flip flop of the IBM reference does not produce output which is an inverse function of the first flip flop plus noise. Please see Figures 3 and 4 of the IBM reference.

Claim 9 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. However, the Examiner failed to provide reasons for which claim 9 was being rejected including the particular part relied upon for the rejection of claim 9. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that claim 9 is not anticipated by the IBM reference for the same reasons for which claim 7 is not anticipated by the IBM reference.

Claim 10 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. However, the Examiner failed to provide reasons for which claim 10 was being rejected including the particular part relied upon for the rejection of claim 10. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 10 for the same reasons for which the IBM reference does not anticipate claim 9. In addition, the IBM reference does not require the circuits be on a single integrated circuit chip as recited by claim 10.

Claim 11 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. However, the Examiner failed to provide reasons for which claim 11 was being rejected including the particular part relied upon for the rejection of claim 11. The Applicant respectfully submits that the IBM reference does not anticipate claim 11 for the following reasons: first, the IBM reference does not teach a plurality of analog circuits as recited by claim 11; second, the IBM reference does not teach a noise separator circuit as recited by the amended claim 11; and, finally, the IBM reference does not teach a noise canceling circuit as recited by claim 11.

Claim 14 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. However, the Examiner failed to provide reasons for which claim 14 was being rejected including the particular part relied upon for the rejection of claim 14. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 14 because, *inter alia*, claim 14 recites a step of supplying a null signal to a second circuit. In contrast, the IBM reference supplies to the second circuit a signal which is not null. Please see signals (A) and (a) of Figures 3 and 4 of the IBM reference.

Claim 15 was rejected under 35 U.S.C. 102(b) as being anticipated by the IBM reference. However, the Examiner failed to provide reasons for which claim 15 was being rejected including the particular part relied upon for the rejection of claim 15. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 15 for the same reasons for which the reference does not anticipate claim 14.

Claim 16 was rejected under 35 U.S.C. 102(b) as being anticipated by IBM reference. However, the Examiner failed to provide reasons for which claim 16 was being rejected including the particular part relied upon for the rejection of claim 16. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 16 for the same reasons for which the IBM reference does not anticipate claim 14. Further, the Applicant respectfully submits that the IBM reference does not anticipate claim 16 because the IBM reference does not identify the step of subtracting said second output from said first output.

Claim 17 was rejected under 35 U.S.C. 102(b) as being anticipated by IBM reference. However, the Examiner failed to provide reasons for which claim 17 was being rejected including the particular part relied upon for the rejection of claim 17. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 17 for the same reasons for which the IBM reference does not anticipate claim 14. Further, the Applicant respectfully submits that the IBM reference does not anticipate claim 17 because the IBM reference does not identify the step of subtracting said second output from said first output.

Claim 19 was rejected under 35 U.S.C. 102(b) as being anticipated by IBM reference. However, the Examiner failed to provide reasons for which claim 19 was being rejected including the particular part relied upon for the rejection of claim 19. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 19 for the same reasons for which the IBM reference does not anticipate claim 14. Further, the Applicant respectfully submits that the IBM reference does not anticipate claim 19 because the IBM reference does not identify the step of subtracting said second output from said first output.

Claim 3 was rejected under 35 U.S.C. 103(a) as being obvious from the IBM reference. However, the Examiner failed to provide reasons for which claim 3 was being rejected including the particular part relied upon for the rejection of claim 3 See 37 CFR 1.104 et seq. and MPEP 707 et seq.

For an obviousness rejection under 35 U.S.C. 103(a), the following three elements are required: (1) suggestion or motivation in the reference to modify the reference; (2) a reasonable expectation of success; and (3) the prior art references must teach or suggest all of the claim limitations. MPEP 2143 et seq. Further, the Examiner must point out the particular parts of the cited references relied upon for the rejection. 37 CFR 1.104 et seq., MPEP 707 et seq. The Applicant respectfully submits that none of these requirements are met, and that the rejections must be withdrawn.

Here, there are no suggestions or motivations to modify the IBM reference to meet the elements of claim 3. The IBM reference states that the goal of its design is to reduce the frequency of the incoming signal for a long distance transmission. "This article describes a solution to a problem concerned with the single transmission of high frequency through a long path." The IBM reference page 3981. In contrast, the present invention discloses a technique for eliminating noise regardless of the frequency. Because of the divergent goals, there are no motivations, within the IBM reference, to eliminate the noise.

Here, there is no showing that the IBM reference would be or can be successfully modified for elimination of noise. Because the goal of the IBM reference is to reduce the frequency of the signal to be transmitted over long distances, the success, as defined by the IBM reference, is the reduction of the frequency of the incoming signal. In contrast, the success, as defined by the present invention, is the reduction of noise. Because the goals of the IBM reference and of the present invention are vastly different, there is no expectation of success as to the IBM reference regarding the goals of the present invention of the elimination of noise.

Most importantly, the IBM reference does not teach all limitations of the elements recited by claim 3. Claim 3 is dependent on claim 1. Here, the IBM reference does not even disclose all of the limitations of claim 1. The first circuit of claim 1 requires a first input and a first output wherein said first output is a function of said first input plus noise. Contrary to the first circuit, the first flip flop of the IBM reference having input (A) and output (B) does not have an output which is a function of its input (A) plus noise component. In fact, the output (B) of the first flip flop of the IBM reference is a function of an input (A) and its own output (B) which is fed back into the first flip flop. Moreover, output (B) has no noise component. As for the second circuit of claim 1, the second flip flop of the IBM reference having input (a) and having output (C) is not required to be located proximal to the first flip flop. And, the second input (a) does not cause the second output (C) to equal the noise component of the first output (B). Moreover, the EXCLUSIVE OR (XOR) gate of the IBM reference is not a subtractor circuit as recited in claim 1. The XOR gate of the IBM reference does not subtract the second output (C) from the first output (B). Thus, the IBM reference does not disclose all the limitations of claim 1. A priori, the IBM reference does not disclose all the limitations of claim 3.

Moreover, the IBM reference does not teach the use of halving circuit as a part of the subtractor circuit. It is inconsistent for the Examiner to claim that "the halving circuit function as a subtractor is notoriously well known in the art" and yet claim that "it is not understood what the halving circuit is and how the subtractor can be the halving circuit." The Office Action, page 4 and page 3.

Claim 8 was rejected under 35 U.S.C. 103(a) as being obvious from the IBM reference. However, the Examiner failed to provide reasons for which claim 8 was being rejected including the particular part relied upon for the rejection of claim 8. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that claim 8 is not obvious from the IBM reference for the same reasons for which claim 3 is not obvious from the IBM reference.

Claim 11 was rejected under 35 U.S.C. 103(a) as being obvious from the IBM reference. However, the Examiner failed to provide reasons for which claim 11 was being rejected including the particular part relied upon for the rejection of claim 11. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 11 because, *inter alia*, not all of the elements of claim 11 are disclosed by the IBM reference. Due to the failure of the Examiner to specify the particular parts of the IBM reference relied upon for the rejection, the Applicant is not able, at this time, to offer a more specific response.

Claim 18 was rejected under 35 U.S.C. 103(a) as being obvious from the IBM reference. However, the Examiner failed to provide reasons for which claim 18 was being rejected including the particular part relied upon for the rejection of claim 18. See 37 CFR 1.104 et seq. and MPEP 707 et seq. The Applicant respectfully submits that the IBM reference does not anticipate claim 18 because, *inter alia*, not all of the elements of claim 18 are disclosed by the IBM reference. Due to the failure of the Examiner to specify the particular parts of the IBM reference relied upon for the rejection, the Applicant is not able, at this time, to offer a more specific response.

CONCLUSION

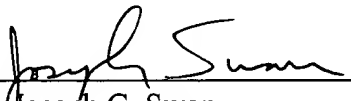
In view of the foregoing amendments and remarks, Applicant respectfully submits that the entire Application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

A Petition for a One-Month Extension of Time and the requisite fee of $110.00 is being filed concurrently herewith. It is not believed that any additional fees are due in connection with the filing of this paper. However, if there are any fees due, including any extensions of time not accounted for above, the Commissioner is hereby authorized to charge such fees to our Deposit Account No. 13-3735. A duplicate copy of this page is attached for that purpose.

Respectfully submitted,

MITCHELL, SILBERBERG & KNUPP LLP

Dated: August 5, 1998

By 
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